REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated October 8, 2002. By the present amendment, the claims have been amended to overcome the 35 U.S.C. 112, second paragraph, rejection. Also, independent claims 1, 9, 12, 15 and 16 have been amended to clarify certain features of the invention. In addition, new claims 17-19 have been added to define the features of the invention regarding extinguishing captured electrons, while new claims 20-26 have been added to define features of the original claims 3, 10-14 and 16 in independent form with amendments to overcome the 35 U.S.C. 112 rejection, but without the further amendments made to claims 1, 9, 12 and 16. By virtue of the fact that claims 3, 10-14 and 16 have not been rejected over prior art, allowance of claims 20-26 which correspond to claims 3, 10-14 and 16, is respectfully requested.

Briefly, the present invention is directed to provide an improved IGFET or an improved imaging display using such an IGFET. More particularly, the present invention is directed to providing an arrangement for TFTs such as those used in imaging display devices, which permits operating such TFTs at reduced power levels.

Figs. 19 and 20A-20C provide an illustration of a prior art arrangement and a problem associated therewith. Fig. 19 shows a typical prior art display device in which pixels 201 each have a pair of TFTs 202 and 203 connected in series with LCD capacitors 204. Fig. 20A shows a typical prior art TFT used in such an imaging device. As shown there, the TFT includes source regions 221 and 222 having a first conductivity type and drain regions 223 and 224 of the same conductivity type, with a

channel region 225 interposed between the source and drain, and a gate electrode 220 overlapping the entire length of the channel 225. Fig. 20B shows an ideal characteristic for such a TFT in which electrons flow smoothly from the source to the drain when the proper voltages are applied to the source and drain. The right-hand side of Fig. 20B also shows an ideal characteristic for the TFT in which the current Ids becomes quite high for a relatively low voltage Vgs.

Fig. 20C, on the other hand, shows an example of a real characteristic which typically occurs with prior art devices such as shown in Fig. 20A. In particular, this shows captured carriers 231 at potential barriers 230 caused by crystal defects and grain boundaries. In comparison with the ideal characteristics of Ids shown in Figs. 20B, in Fig. 20C, one can see the need for a much higher Vgs for a high Ids in the real case compared with the ideal case. In other words, the captured carriers cause such an increase in the necessary voltage Vgs, as discussed on page 6, line 6 et seq. In particular, typically 10-15 volts are actually required.

The purpose of the present invention is to reduce the carrier capture levels so that TFTs can operate closer to the ideal situation and, correspondingly, so that the gate voltages Vgs can be reduced (e.g. see page 7, line 5 et seq.). To do this, a portion of the channel 24 is arranged so that it is not overlapped by a gate electrode 20. The area free from being overlapped by the gate electrode can be longer than the crystal grain size of the polysilicon forming channel 24 (e.g. see page 7, line 18 et seq.).

Figs. 3A-3C show an example of an embodiment of the present invention that can provide the improved low voltage operation sought by the present invention. As can be seen in Fig. 3A, the structure of the embodiment provides a first source region 22 of a first conductivity type and a second source region 23 of a second

conductivity type different than the first conductivity type. In addition, the gate electrode 20 only overlaps a portion of the channel 24 between the two sources so that another portion of the channel 24 is not overlapped by the gate.

Referring to Fig.3B and the description on page 16 et seq., the electrons injected from the source 22 into the channel 24 are subject to being captured by the potential barrier 30. However, by virtue of the structure shown in Fig. 3A, holes can be injected by the source 23 to provide a recombination center that effectively extinguishes the captured electrons 25 shown in Fig. 3B. Accordingly, the problem with captured electrons is greatly reduced. As a result, the Ids characteristic of the device is much closer to that shown in the ideal Fig. 20B, and the device can operate to significantly reduce power.

Reconsideration and allowance of claims 1, 6, 8 and 9 over Jambotkar and claims 1, 2, 4, 5, 7 and 15 over Ohkubo is respectfully requested. By the present amendment, claims 1, 9, 12, 15 and 16 have been amended to define a single channel between the first and second conductivity type source areas in conjunction with the non-overlapped area portion of the channel region. Thus, an arrangement is defined in which a first type carrier charge (such as an electron or a hole) is moved into the single channel from one source with the gate electrode turned on while a second type carrier charge is moved into the single channel from the other source. Thus, both first and second types of carrier charges exist in the single channel. The first type carrier charge which is trapped at the trap level is then recoupled with the second type carrier charge, resulting in the extinguishing of the charges. As discussed above, this results in an improved device requiring less gate-source voltage.

It is respectfully submitted that nothing in Jambotkar teaches or suggests the

arrangement set forth in these amended independent claims. Jambotkar teaches a CCD structure having two CCD memories arranged on top and bottom, wherein each of the two CCD memories use as a type of carrier charge. In other words, one of the CCD memories uses electrons while the other uses holes. Thus, each of the CCD memories independently uses carrier charges, as discussed on column 2, lines 15 and 16. However, nothing in Jambotkar teaches or suggests the claimed features of having a first and a second source area of different conductivity types from one another in conjunction with a single channel formed between the first and second conductivity type source areas, together the with claimed feature of a portion of the single channel not being overlapped by a gate electrode. Therefore, reconsideration and allowance of these amended claims over Jambotkar is respectfully requested.

Similarly, Ohkubo discloses a p-type region which is not a source type region, but is, instead, a p-type substrate used for a monocrystal Si-nMOS transistor. When the gate of this transistor is turned off, a channel surface goes into an accumulation state by supplying holes from the p-type substrate. Generally, there is no p-type substrate for an nMOS TFT, so there is no hole supply source. Accordingly, Ohkuko provides such a p-type region which becomes a hole supply source, as described on column 3, lines 8-13. Thus, the p-type region of Ohkubo is not a source region, and, correspondingly, this reference fails to teach or suggest the features of the amended independent claims 1, 9, 12, 15 and 16 over first and second source regions of different conductivity type operating in conjunction with a single channel in which a portion of the channel is not overlapped a gate electrode. Therefore, reconsideration and allowance of independent claims 1, 9, 12, 15 and 16 over Ohkubo is also respectfully requested.

Consideration and allowance of the newly submitted claims 17-19 is also

respectfully requested. As noted above, these claims are particularly directed to defining the invention including means for extinguishing captured electrons injected from the first source into the channel region, which captured electrons have been captured by potential barriers between the channel regions. Claim 18 more specifically defines the extinguishing means in terms of providing a gate electrode in a manner so as not to overlap a portion of the channel region. It is respectfully submitted that nothing in the cited references to Jambotkar or Ohkubo teach or suggest such an extinguishing means. Therefore, consideration and allowance of independent claim 17 and its dependent claims 18 and 19 over these references is also respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.40674X00).

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1-16 have been amended as follows:

1. (Amended) An insulated gate field effect transistor having a gate electrode [in] overlapping a channel area between a first conductivity type source area and a second conductivity [types] type [of] source [areas] area thereof, wherein:

said channel area provides a single channel between said first and second conductivity type source areas and includes a non-overlapped [comprises an] area portion free from being overlapped by [lapping over] the gate electrode in plan.

2. (Amended) The field effect transistor according to claim 1, wherein:

said channel area is [made] comprised of a polycrystal silicon film.

3. (Amended) The field effect transistor according to claim 2, wherein:

the non-overlapped area portion of said channel area [free from lapping over the gate electrode in plan] has a length longer than a crystal grain size of the polycrystal silicon that [composes] comprises said channel area.

4. (Amended) The field effect transistor according to claim 1, wherein:

said channel area is [made] comprised of an intrinsic semiconductor.

5. (Amended) The field effect transistor according to claim 4, wherein:

the non-overlapped area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

6. (Amended) The field effect transistor according to claim 1, wherein:

said gate electrode is provided on an opposite side of a substrate, which [holds] includes said channel area, from said channel area.

7. (Amended) The field effect transistor according to claim 1, wherein:

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said gate electrode is provided between said channel area and [said] a substrate that [holds] includes said channel area.

8. (Amended) The field effect transistor according to claim 1, wherein:

at least a part of said gate electrode [laps] overlaps [over] one of said first and second source areas in plan.

9. (Amended) An insulated gate type field effect transistor having a gate electrode [in] overlapping a channel area between a first conductivity type source area and a second conductivity [types] type [of] source [areas] area thereof, wherein:

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said channel area provides a single channel between said first and second source areas and said gate electrode comprises two separate subgate electrodes disposed on [the] respective sides of said first and second conductivity [types] type [of] source areas in a direction in which said channel area extends.

10. (Amended) The field effect transistor according to claim 9, wherein:

said channel area is [made] comprised of an intrinsic semiconductor.

11. (Amended) The field effect transistor according to claim 10, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

12. (Amended) A double field effect transistor device of an insulated gate type, comprising:

a channel area taking a virtually H-type form in plan;

a first pair of source areas different in [conductive] conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that [composes] comprises a part of the H, wherein a first single channel is provided in said channel area coupling between both of said first pair of source areas;

a second pair of source areas different in [conductive] conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that [composes] comprises a part of the H so that the source areas formed respectively at the ends of said pair of parallel strips extending in the same direction are different in [conductive] conductivity type, wherein a second single channel is provided in said channel area coupling between both of said second pair of source areas; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that [composes] comprises a part of the H and a central link of the H that combines said pair of parallel strips.

13. (Amended) The field effect transistor according to claim 12, wherein:

said channel area is [made] comprised of an intrinsic semiconductor.

14. (Amended) The field effect transistor according to claim 13, wherein:

the channel area includes a non-overlapped area portion free from being overlapped by the gate electrode in plan and the area portion of said channel area contains injected impurities of less than 1 $e^{-}18/cm^{3}$.

15. (Amended) An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein[.]:

at least part of said controller is comprised of an insulated gate type field effect transistor having a gate electrode [in] overlapping a channel area between a first conductivity type source area and a second conductivity [types] type [of] source [areas] area thereof; and

said channel area includes a non-overlapped [comprises an] area portion free from [lapping over] being overlapped by the gate electrode in plan.

16. (Amended) An image display apparatus comprising a display unit of a plurality of pixels formed on an insulating substrate, and a controller formed on the insulating substrate for at least processing a display signal and for writing the display signal to said display unit, wherein[.]:

at least part of said controller is comprised of an insulated gate type field effect transistor having a gate electrode [in] overlapping a channel area between a first conductivity type source area and a second conductivity source [areas] area thereof; and

said channel area [comprises an] includes a non-overlapped area portion free from [lapping over] being overlapped by the gate electrode in plan; and said apparatus comprising:

an image control unit of said display unit being of an insulated gate type, said image control unit comprising:

a channel area taking a virtually H-type form;

a first pair of source areas different in [conductive] conductivity type from one another respectively formed at opposite ends of one of a pair of parallel strips that [composes] comprises a part of the H, wherein a first single channel is provided in said channel area coupling between both of said first pair of source areas;

a second pair of source areas different in [conductive] conductivity type from one another respectively formed at opposite ends of the other of said pair of parallel strips that [composes] comprises a part of the H so that the source areas

formed respectively at the ends of said pair of parallel strips extending in the same direction are different in [conductive] conductivity type, wherein a second single channel is provided in said channel area coupling between both of said second pair of source areas; and

a gate electrode lapping over an area of the H that comprises the central portions of said pair of parallel strips that [composes] comprises a part of the H and a central link of the H that combines said pair of parallel strips.

New claims 17 – 26 have been added.